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FUZZY BASED BRIDGELESS DC TO DC CONVERTER WITH IMPROVED POWER FACTOR

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ABSTRACT

Dc link stabilization has been done with two stage conversion, in order to improve the power factor at delivery point. This project presents a novel ac/dc converter and further DC to Ac converter with a 3 phase load based on a quasi-active power factor correction (PFC) scheme. In the proposed Simulink model, the power factor is improved by using an auxiliary winding coupled to the transformer of a cascade dc/dc flyback converter. The auxiliary winding is placed between the input rectifier and the low-frequency filter capacitor to serve as a magnetic switch to drive an input inductor. Since a rectifier and subsequent stage of the dc/dc converter is operated at high-switching frequency, the auxiliary windings produce a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. It eliminates the use of active switch and control circuit for PFC, which results in lower cost and higher efficiency. In order to prove the simulation results, a tiny section of hardware using a micro controller based DC stabilization using PWM pulses. The program is written in any pc in a notepad file and assembled using ASEM 5113. A flash programmer is used to burn the hex file into the controller. The performance is verified using CRO and a multimeters.

INTRODUCTION

Stability problems of electric power systems containing constant power loads (CPLs) are well known and have been reported in, for example, automotive, aerospace, marine, and traction applications [1]–[5]. The origin of these problems is that the constant power characteristics (with respect to dc-link voltage variations) make CPLs behave like incremental negative resistances, which reduce damping of the feeding systems and may cause instability. Although the CPL, in general, can be fed through a converter or a passive circuit (see [6] for an overview of different topologies), this contribution exclusively considers CPLs fed by ideal dc supplies through passive LC filters. In order not to reduce efficiency or increase the filter complexity, passive stabilization by modifying the physical input filter as proposed in [7] and [8] is not considered, and since the power source is assumed uncontrollable, methods modifying the supply voltage as described in [9]–[12] are not applicable. Consequently, it remains to actively stabilize the system by modifying the power consumed by the CPL.

Conventional offline power converters with diode– capacitor rectifiers have resulted in distorted input current waveforms with high harmonic contents. To solve these problems, so as to comply with the harmonic standards such as IEC 61000-3-2, several techniques have been proposed to shape the input current waveform of the power converter. A common approach to improving the power factor is a two-stage power conversion approach. The two-stage scheme results in high power factor and fast response output voltage by using two independent controllers and optimized power stages. The main drawbacks of this scheme are its relatively higher cost and larger size resulted from its complicated power stage topology and control circuits, particularly in low power applications. In order to reduce the cost, the single-stage approach, which integrates the PFC stage with a dc/dc converter into one stage, is developed.

These integrated single-stage power factor correction (PFC) converters usually use a boost converter to achieve PFC with discontinuous current mode (DCM) operation. Usually, the DCM operation

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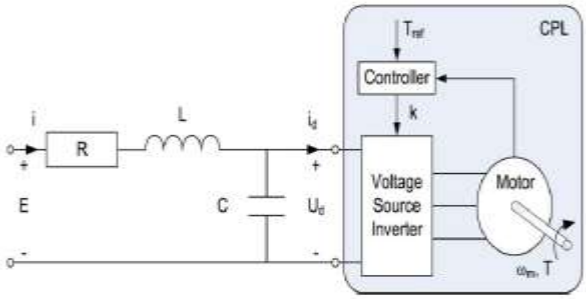
gives a lower total harmonic distortion (THD) of the input current compared to the continuous current mode (CCM). However, the CCM operation yields slightly higher efficiency compared to the DCM operation. Generally, single-stage PFC converters meet the regulatory requirements regarding the input current harmonics, but they do not improve the power factor and reduce the THD as much as their conventional two-stage counterpart. The power factor could be as low as 0.8, however, they still meet the regulation.

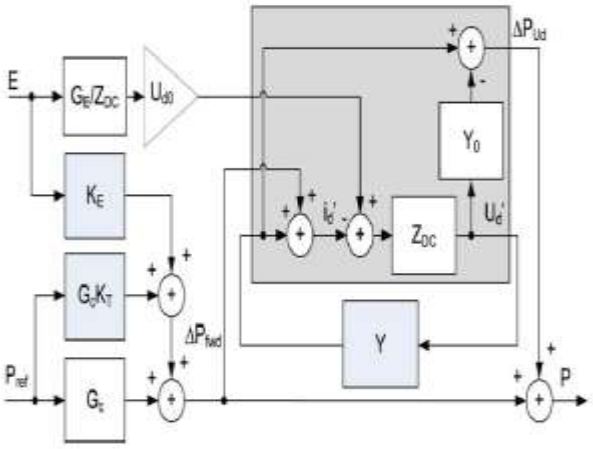
In addition, although the single-stage scheme is especially attractive in low cost and low power applications due to its simplified power stage and control circuit, major issues still exist, such as low efficiency and high as well as wide-range intermediate dc bus voltage stress. To overcome the disadvantages of the single-stage scheme, many converters with input current shaping have been presented, in which a high frequency ac voltage source (dither signal) is connected in series with the rectified input voltage in order to shape the input current. However, the harmonic content can meet the regulatory standard by a small margin. In, a new concept of quasi-active PFC is proposed to improve the efficiency of a single-stage converter by preventing the input current or voltage stress due the PFC cell from being added to the active switch. In this, the dc/dc cell operates in DCM so that a series of discontinuous pulses is used to shape the input inductor current and the PFC is achieved. As the circuit uses resonance of circuit parameters to achieve PFC, the control of the power factor will be very sensitive to the variation of components values.

EXISTING SYSTEM

A CPL connected to an ideal power supply via an input LC filter is shown in Fig. 1. In the figure, the general CPL is exemplified by a motor drive with four induction motors in parallel, which will be used as a test system in this paper.

The LC filter and induction motors are characterized by the following data:





Although power modifications as functions of the dc-link voltage directly modify the load input admittance, stabilization based on other quantities like the inductor current has also been suggested. As the inductor current can be represented as a linear combination of dc-link and supply voltages, such stabilization is related to the method suggested in [16], using exactly these inputs to simulate virtual resistance in parallel with the filter inductor. The supply voltage is considered as an ideal external input (independent of the line current), and these methods therefore can be regarded as two degrees of freedom controllers, where the dc-link voltage feedback stabilizes the system and the feed forward component from the supply voltage facilitates a means to possibly reduce the power disturbance. Based on this observation, it is natural to consider also the other external excitation signal of the LC

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filter for feed forward control, i.e., the dc-link current. This quantity depends on the dc-link voltage and the load power Since the power, in turn, is affected by variations of the power reference through an assumed closed-loop transfer function GC (and possibly various disturbances that are neglected here), the following very general stabilization control law was introduced, which also is applied here.

PROPOSED SYSTEM

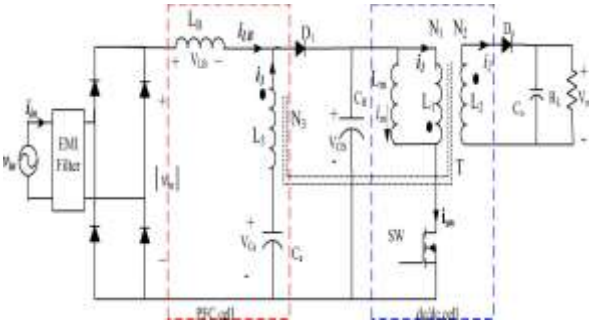


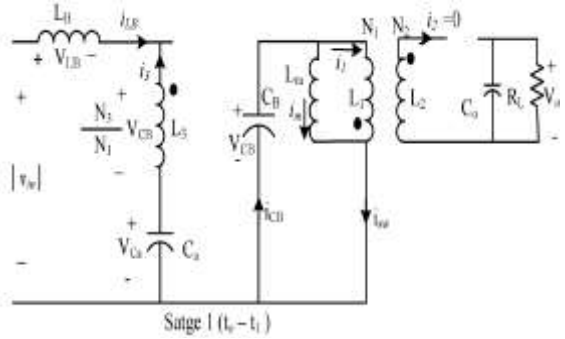
Figure. Two state Ac to DC converter

In this project, a new technique of quasi-active PFC is proposed. The PFC cell is formed by connecting the energy buffer (*LB*) and an auxiliary winding (*L*3) coupled to the transformer of the dc/dc cell, between the input rectifier and the low-frequency filter capacitor used in conventional power converter. Since the dc/dc cell is operated at high frequency, the auxiliary winding produces a high frequency pulsating source such that the input current conduction angle is significantly lengthened and the input current harmonics is reduced. The input inductor *LB* operates in DCM such that a lower THD of the input current can be achieved. The proposed quasi-active PFC circuit is analyzed in this section. The circuit comprised of a bridge rectifier, a boost inductor *LB* , a bulk capacitor *Ca* in series with the auxiliary windings *L*3 , an intermediate dc-bus voltage capacitor *CB* , and a discontinuous input current power load, such as flyback converter.

The flyback transformer (*T*) has three windings *N*1, *N*2, and *N*3. The secondary winding *N*2 = 1 is assumed. In the proposed PFC scheme, the dc/dc converter section offers a driving power with high-frequency pulsating source. The quasi active PFC cell can be considered one power stage but without an active switch.

VARIOUS OPERATING STAGES:

STAGE1:



When the switch (SW) is turned on at $t = to$, diodes *D*1 and *Do* are OFF, therefore, the dc-bus voltage *VCB* is applied to the magnetizing inductor *Lm*, which causes the magnetizing current to linearly increases. This current can be expressed as,

$$i_m = \frac{V_{CB}}{L_m}(t_o - t_1).$$

And since diode *D*1 is OFF, the input inductor *LB* is charged by input voltage, therefore, the inductor current *iLB* is linearly increased from zero since it is assumed that the PFC cell operates in DCM. This current can be expressed as,

$$i_{LB} = \frac{|V_{in}| + (N_3/N_1)V_{CB} - V_{Ca}}{L_B}(t_o - t_1)$$

where, *V*in = *Vm*| sin θ| is the rectified input voltage, (*to* − *t*1) = *dTS* is the ON-time of the switch (SW), *LB* is the boost inductor and *N*1 , *N*3 are the primary and auxiliary turns ratio, respectively. At this stage, *iLB* = −*i*3 and the capacitor *Ca* is in the charging mode. On the other hand, *Do* is reversed biased and there is no current flow through the secondary winding. Therefore, it can be seen that the magnetizing current *im* is supplied by the discharging current from the dc bus capacitor *CB* and the current *i*3 which is equal to input current *iLB* at this stage. The current through the main switch (SW) is given by

$$i_{SW} = i_{CB} = i_m - \frac{N_3}{N_1}i_3 = i_m + \frac{N_3}{N_1}i_{LB}.$$

Therefore, the current stress of the switch can be reduced by selecting the turns ratio (*N*3/*N*1),

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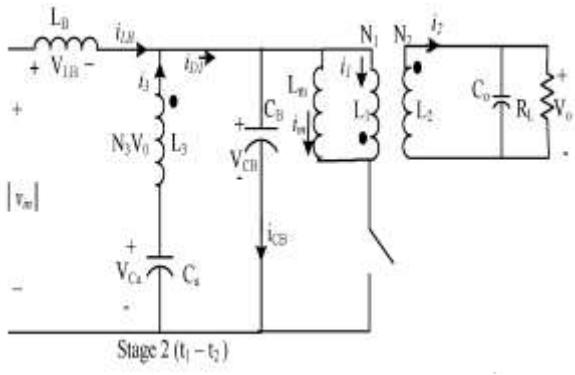
which is designed to be less than 1 to ensure proper operation of the transformer. Compared to the single-stage BIFRED converter [11], the switch current is given by

$$i_{SW} = i_m + i_{LB}.$$

Obviously, the proposed circuit has less switch current stress, therefore, the conduction loss and switching losses are reduced, and the efficiency is improved correspondingly. This stage ends when the switch is turned off at $t = t1$.

STAGE2:



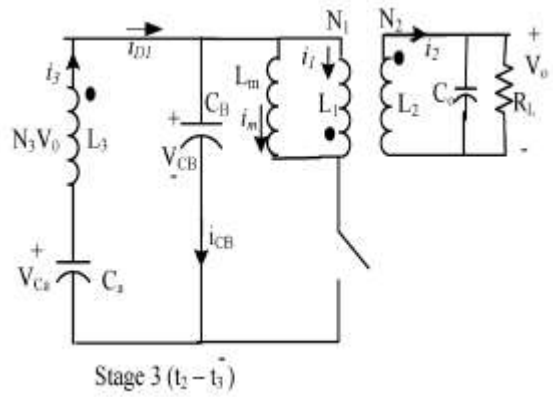
When the switch is turned OFF at $t = t1$, output diode *Do* begins to be forward biased. Therefore, the energy stored in the transformer magnetizing inductor is delivered to the load through the secondary winding. Similarlythe diode *D*1 is also forward biased and the voltage across *LB* now*V*in − *VCB*. Therefore, the current *ILB* is linearly decreased to zero at $t = t2$ (DCM operation), and the energy stored in *LB* is delivered to the dc bus capacitor *CB* . Therefore

$$i_{LB} = \frac{|V_{in}| - V_{CB}}{L_B}(t_1 - t_2).$$

The capacitor (*Ca*) is also discharging its energy to the dc bus capacitor *CB* and the current *i*3 reverse its direction. Therefore, the capacitor current is given by,

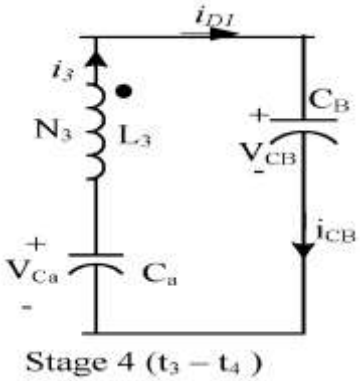
$$i_{D1} = i_{CB} = i_{LB} + i_3$$

STAGE3:



At this stage, the input inductor current *iLB* reaches zero and the capacitor *Ca* continues to discharge its energy to the dc bus capacitor *CB* . Therefore, *iD*1 = *iCB* = *i*3 . At $t = t3$, the magnetizing inductor releases all its energy to the load and the currents *im* and *i*2 reach to zero level because a DCM operation is assumed.

STAGE4:



This stage starts when the currents *im* and *i*2 reach to zero. Diode*D*1 still forward biased, therefore, the capacitor *Ca* still releasing its energy to the dc bus capacitor *CB* . This stage ends when the capacitor *Ca* is completely discharged and current *i*3 reaches zero. At $t = t5$, the switch is turned on again to repeat the switching cycle.

SWITCHING WAVEFORMS

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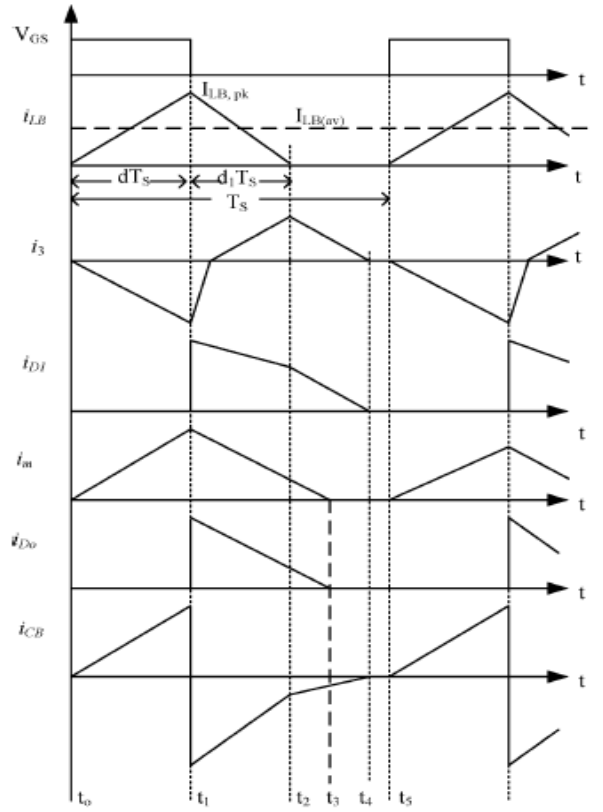

OUTPUTS

Simulink model

DC link with PFC correction

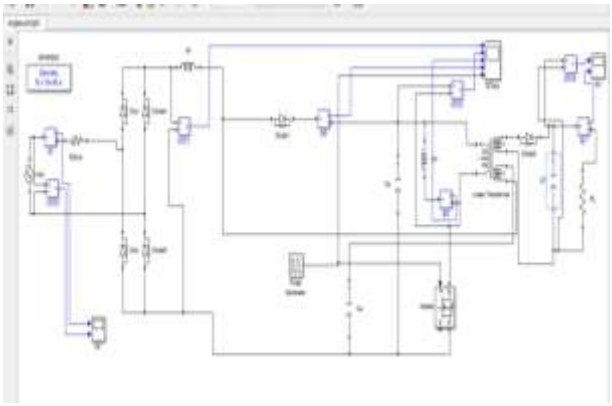

Fig: Proposed Simulink model

The proposed Simulink model performed with discrete powergui at a sampling rate of $5e^{-6}$ s. Input mains voltage is first rectified with an uncontrolled rectifier using rectifier blocks and applied to energy storing devices such as inductor and capacitor. A mosfet block is used to switch the rectified DC and the switched power is coupled to the DC load via a multi-tapped SMPS transformer. The level of DC is sensed via an another coil of the secondary and fed back to the input section in order to identify the current phase. This feedback reduces the phase lag in current and increases the power factor. DC load is in the order of 100 ohms.

Input side I and V

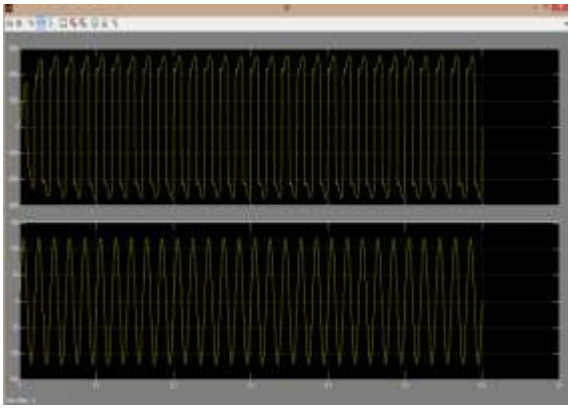

Fig: Current and voltage waveform at input AC side

Output DC voltage and DC current

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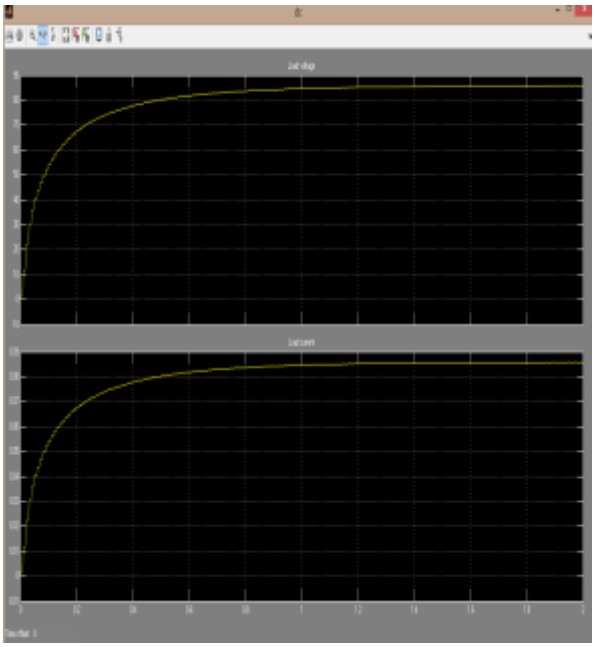
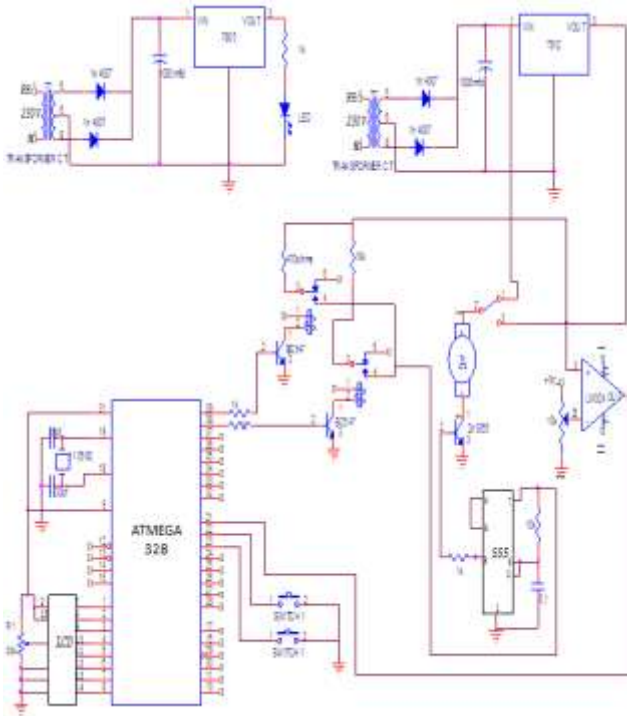
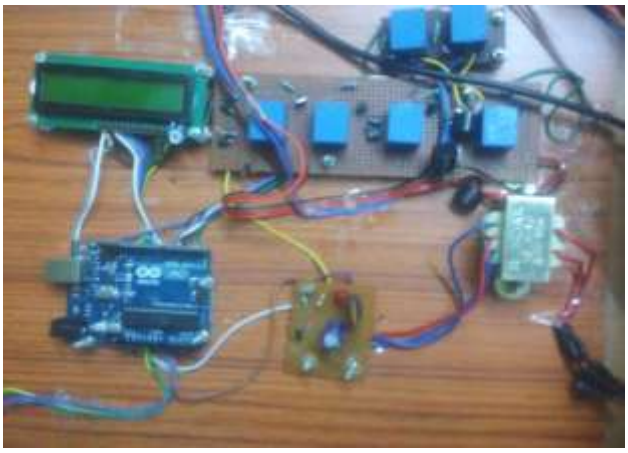


Fig: DC voltage and current at DC load side

HARDWARE IMPLEMENTATION



SNAPSHOT OF THE HARDWARE



CONCLUSION

In this project, a new ac/dc converter based on a quasi-active PFC scheme has been presented. The proposed method produces a current with low harmonic content to meet the standard specifications as well as high efficiency. This circuit is based on adding an auxiliary winding to the transformer of a cascade dc/dc DCM fly back converter. The input inductor can operates in DCM to achieve lower THD and high power factor. By properly designing the converter components, a tradeoff between efficiency and harmonic content can be established to obtain compliance with the regulation and efficiency as high as possible. In addition to the simulation, a hardware implementation has been realized using ATMEGA 328 on the Arduino Uno board.

Parameters	Existing system	Proposed system
Harmonics	5%	2.2%
Power factor	0.98	0.99

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